REMARKS

Claims 1-15 are pending. By this amendment, claim 1 is amended.

The Office Action rejects claims 1-14 under the judicially created doctrine of obviousness type double patenting over claims 1-14 of related applications 10/614,859, 10/614,860, 10/614,861, 10/614,862 and 10/614,863. It is submitted that this rejection for each of these applications should be provisional, until one of the applications is otherwise ready to issue. That application should then be allowed to issue, and the double patenting rejection, if still in affect, should be made non-provisional, and applicants will then consider whether to submit a terminal disclaimer.

The Office Action rejects claims 1-15 under 35 USC 103 over O'Brien (US Pat. 5,247,638) in view of Totani (US Pat. 5,175,842). This rejection is respectfully traversed.

Claim 1 of the application recites a storage system that includes at least one first processor controlling transfer of data between said control unit and said plurality of cache units, and at least one second processor controlling transfer of data between said control unit and said plurality of cache units. In addition, other elements of the present invention allow transfer of data between the channel unit and the cache units to be executed in parallel. Accordingly, both the process of reading/writing data related to the host computer from/to the cache unit and the process of reading/writing between the cache unit and the disk device can be executed efficiently.

In contrast, as shown in Fig. 2 etc. of O'Brien, the transfer of data between the multipath storage director 110 and the cache 113 and the transfer of data between the cache 113 and the cluster control 111 of the disk drive manager 102 are controlled only by processor IUP204 by using the control bus 206-C. Thus, O'Brien does not disclose at least one first processor controlling transfer of data between said control unit and said plurality of cache units, and at least one second processor controlling transfer of data between said control unit and said plurality of cache units.

Totani does not solve these deficiencies of O'Brien. In Totani, only the memory control unit 2 is disposed among the host computer 1, the plurality of caches 8 and 9, and the external memory unit 3 to transfer data. So, Totani also does not disclose or suggest at least one first processor controlling transfer of data between said control unit and said plurality of cache units, and at least one second processor controlling transfer of data between said control unit and said plurality of cache units, as required by claim 1 of the application.

Accordingly, because neither applied reference discloses or suggests these features, even if combined as suggested, the applied references would not have rendered obvious claim 1, or dependent claims 2-15 of the application. Accordingly, it is requested that the rejection under 35 USC 103 be withdrawn.

For the above reasons, it is submitted that the application is in condition for allowance. A Notice of Allowance in due course is solicited. The Office is hereby authorized to charge any additional fees under 37 C.F.R. §1.16, §1.17, or §1.136 or credit any overpayment to Deposit Account No. 11-0600.

Should the Examiner have any questions concerning this matter, he is invited to contact Applicants' undersigned attorney at 202/220-4334.

Respectfully submitted,

Date: February 22, 2005

David J. Zibelli
Registration No. 36,394

KENYON & KENYON
1500 K Street, N.W. - Suite 700
Washington, D.C. 20005-1257
Tel: (202) 220-4200
Fax: (202) 220-4201

548771_DC01